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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,421	10/01/2003	Gee-Sung Chae	8734.241.00 US	5657

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EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,421	CHAE ET AL.	
	Examiner	Art Unit	
	WILLIAM L. BODDIE	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,10 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,10 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, January 28th, 2009 the Applicant amended claims 1 and 10. Currently claims 1, 4 and 10-11 are pending.

Response to Arguments

2. Applicant's arguments filed January 28th, 2009 have been fully considered but they are not persuasive.

3. On page 5 of the Remarks, the Applicants argue that Shin does not teach the newly added claim limitation. There is never any consideration of the combination of Shin and Sakamoto.

4. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). This is particularly true, as in the current case, the combination of the art teaches the newly added limitation.

In short, as the rejection is fully described below in the updated rejection, Sakamoto teaches placing the common electrode on the passivation layer, but not on the same layer as the pixel electrode. Shin discloses, placing the common electrode on the same layer as the pixel electrode. Therefore it would seem obvious to one of ordinary skill in the art to place Sakamoto's pixel electrode on the passivation layer alongside the common electrode.

As such the rejection is seen as sufficient and is maintained.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 4 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al. (US 6,069,678) in view of Shin et al. (US 6,356,328) and further in view of Lee (US 6,459,465).

With respect to claim 1, Sakamoto discloses, an in-plane switching mode liquid crystal display device, comprising:

a plurality of gate lines (105 in fig. 24) and data lines (205 in fig. 24) defining a plurality of pixels;

a thin film transistor (505 in fig. 24) in each of the pixels, the thin film transistor including a gate electrode (1405 in fig. 25) on a substrate (605 in fig. 25), an insulating layer (2405 in fig. 25) over the gate electrode, a semiconductor layer (1105, 2505 in fig. 25) on the insulating layer, a source electrode (1005 in fig. 25) and a drain electrode (905 in fig. 25) on the semiconductor layer;

a common line (part of 305 in fig. 24 that runs horizontally);

at least one pixel electrode (405 in fig. 24) having a predetermined width (clear from fig. 6) in each of the pixels; and

at least one common electrode (305 in fig. 24) having a predetermined width (Wcom in fig. 24) completely overlapping a data line (205 in fig. 24) in width (clear from

fig. 24), the common electrode being substantially parallel to the pixel electrode (seems again clear from fig. 24) and the common electrode being alternately disposed with the pixel electrode (seems clear from fig. 24, that the common and pixel electrodes alternate);

a passivation layer (2605 in fig. 25) over the source electrode, drain electrode and semiconductor layer, and

wherein the common electrode is disposed on the passivation layer (col. 10, lines 45-46; also note fig. 26).

Sakamoto does not expressly disclose, that the common electrode is connected to the common line, on the substrate, through a contact hole, nor that the common and pixel electrodes are disposed on the same layer.

Shin discloses, wherein a pixel electrode (16b in fig. 4) and a common electrode (15b in fig. 4) are disposed on the same layer (fig. 4), a common electrode (15b in fig. 3) and a common line (15a in fig. 3) on a substrate (col. 3, lines 13-14) are disposed on layers different from each other (col. 3, lines 6-14, 34-36) so that the common electrode is connected to the common line through a contact hole (C in fig. 3),

wherein the common electrode and the common line are not overlapped (clear from fig. 3) with a pixel electrode (16b in fig. 3) and the common line is separated a predetermined distance from the end portion of the pixel electrode (clear from fig. 3).

Shin and Sakamoto are analogous art because they are both drawn to structural components of LCD pixels.

At the time of the invention it would have been obvious to dispose the pixel and common electrodes on the same layer and to connect the common line and electrodes of Sakamoto via a contact hole as taught by Shin.

The motivation for doing so would have been to improve aperture ratio and brightness (Shin; col. 2, lines 16-22).

To further explain, Sakamoto discloses placing the common electrode on the passivation layer. Shin discloses placing both the common and pixel electrodes on the same layer. Therefore it seems obvious to place the pixel electrode on the same layer as the common electrode in the Sakamoto embodiment. Upon such a combination, both the pixel and common electrode will be disposed on the passivation layer.

Neither Sakamoto nor Shin expressly disclose that the passivation layer is made of an organic material including BCB and photoacryl.

Lee discloses, a passivation layer is made of an organic material including at least one material of BCB and photoacryl (col. 8, lines 43-50).

Lee, Shin and Sakamoto are analogous art because they are all from the same field of endeavor namely, LCD pixel design and manufacture.

At the time of the invention it would have been obvious to one of ordinary skill in the art to use the organic material taught by Lee to form the passivation layers of Shin and Sakamoto.

The motivation for doing so would have been the well known advantage of providing good flatness characteristics and low permittivity.

With respect to claim 4, Sakamoto, Shin and Lee disclose, the device of claim 1 (see above).

Sakamoto further discloses, wherein the data lines (905 in fig. 25/ 205 in fig. 24) are formed on the insulating layer (2405 in fig. 25).

With respect to claim 10, Sakamoto discloses, an in-plane switching mode liquid crystal display device, comprising:

a plurality of gate lines (105 in fig. 24) and data lines (205 in fig. 24) defining a plurality of pixels;

a thin film transistor (505 in fig. 24) in each pixel, the thin film transistor including a gate electrode (1405 in fig. 25) on a substrate (605 in fig. 25), an insulating layer (2405 in fig. 25) over the gate electrode, a semiconductor layer (1105, 2505 in fig. 25) on the insulating layer, a source electrode (1005 in fig. 25) and a drain electrode (905 in fig. 25) on the semiconductor layer, and a passivation layer over the source electrode, drain electrode and semiconductor layer (2605 in fig. 25),

a common line (part of 305 in fig. 24 that runs horizontally);

at least one pixel electrode (405 in fig. 24);

a first common electrode (left electrode; 305 in figs. 24/27) completely overlapping a data line (205 in figs. 24/27) in width; and

at least one second common electrode in each pixel (center portion electrode in fig. 24), the second common electrode connected to the common line (clear from fig. 24 that the common line is connected to the common electrode),

wherein the pixel electrode has a predetermined width and is substantially parallel to the first and second common electrodes (clear from fig. 24) and **the common electrode is disposed on the passivation layer (col. 10, lines 45-46; also note fig. 26),** the pixel electrode is disposed between the first and second common electrodes and between the second common electrodes (seems clear from fig. 24 that the source electrode is so positioned).

Sakamoto does not expressly disclose, that the common electrode is connected to the common line, on the substrate, nor that the common and pixel electrodes are disposed on the same layer.

Shin discloses, **wherein a pixel electrode (16b in fig. 4) and a common electrode (15b in fig. 4) are disposed on the same layer (fig. 4),** a common line (15a in fig. 3) on a substrate

wherein a common electrode (15b in fig. 3) and the common line are not overlapped (clear from fig. 3) with a pixel electrode (16b in fig. 3) and the common line is separated a predetermined distance from the end portion of the pixel electrode (clear from fig. 3).

Shin and Sakamoto are analogous art because they are both drawn to structural components of LCD pixels.

At the time of the invention it would have been obvious to dispose the pixel and common electrodes on the same layer and to connect the common line and electrodes of Sakamoto via a contact hole as taught by Shin.

The motivation for doing so would have been to improve aperture ratio and brightness (Shin; col. 2, lines 16-22).

To further explain, Sakamoto discloses placing the common electrode on the passivation layer. Shin discloses placing both the common and pixel electrodes on the same layer. Therefore it seems obvious to place the pixel electrode on the same layer as the common electrode in the Sakamoto embodiment. Upon such a combination, both the pixel and common electrode will be disposed on the passivation layer.

Neither Sakamoto nor Shin expressly disclose that the passivation layer is made of an organic material including at least one material of BCB and photoacryl.

Lee discloses, a passivation layer is made of an organic material including at least one material of BCB and photoacryl (col. 8, lines 43-50).

Lee, Shin and Sakamoto are analogous art because they are all from the same field of endeavor namely, LCD pixel design and manufacture.

At the time of the invention it would have been obvious to one of ordinary skill in the art to use the organic material taught by Lee to form the passivation layers of Shin and Sakamoto.

The motivation for doing so would have been the well known advantage of providing good flatness characteristics and low permittivity.

With respect to claim 11, Sakamoto, Shin and Lee disclose, the device of claim 10 (see above).

Sakamoto further discloses, wherein a width of the first common electrode is larger than that of the second common electrode (clear from fig. 24).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM L. BODDIE whose telephone number is (571)272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/William L Boddie/
Examiner, Art Unit 2629
6/1/09